EXHIBIT B

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,530	11/30/2001	Paul L. Master	046301-002000	6090

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EXAMINER
ALROBAYE, IDRISS N

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
09/25/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/997,530	MASTER ET AL.	
	Examiner	Art Unit	
	IDRISS N. ALROBAYE	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *182-305* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *182-305* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/09/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. *attached* .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to applicant's restriction/election filed on 6/22/2009.

2. Claims 182-305 presented for examination. Claims 1-181 are canceled.

Election/Restrictions

3. In response to notice of non-compliant mailed to applicant's on 2/20/2009, applicant's filed amendments on 6/22/2009 reinstated the original claims presented in the case. However, the original claims were canceled and introduced as new claims which still within the scope of the original invention. Thus, the new claims presented in the amendments have been considered and examined.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 182-246, 248-276, 278-305 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise U.S. Patent No. 5,768,561 (hereinafter Wise) in view of Baxter U.S. Patent No. 5,794,062 (hereinafter Baxter).

6. As per claim 182, Wise teaches a system for adaptive configuration, the system comprising:

a first computational unit (see Wise, Fig. 137, resolving adder at the y input) having a configurable basic architecture including a first plurality of heterogeneous computational elements (see Wise, Fig. 137, carry-save multiplier, carry save adder, carry save subtractor) and a first interconnection network configurably coupling the first plurality of heterogeneous computational elements together (Wise, see first common block in Fig. 137), the first interconnection network configuring interconnections between the first plurality of heterogeneous computational elements in response to the first configuration information to perform a basic computational function (see Wise, Fig. 137 and col. 262, lines 14-42); and

a second computational unit (see Wise, Fig. 137, the d multiplier at the x) having a configurable complex processing architecture (see Wise, dynamic adaptive configuration, col. 6, lines 57-67 and col. 7, lines 1-12, complex multiplication) including a second plurality of heterogeneous computational elements (see Wise, x[2,5] of Fig. 37, when reconfigure in a second functional mode which includes, carry save multiplier, carry save subtractor, carry save adder) and a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together (see Wise, second common blocks of Fig. 37 when functioning in a second mode x[2,5]), the second interconnection network configuring interconnections between the second plurality of heterogeneous computational elements in response to the second configuration information to perform a complex processing function (see Wise, Fig. 37 and col. 262, lines 14-42; see also multiplexing circuit in fig. 137).

Wise did not specifically show a memory adapted to store first configuration information and second configuration.

However, Baxter taught a memory for storing first configuration information and a second configuration information (see Baxter, Fig. 4 and 3A for detail configuration sets). It would have been obvious to one of ordinary skill in the relevant art at the time of the invention was made to use Baxter in the invention of Wise of having a memory for storing the first configuration and a second configuration as claimed for the purpose of providing Wise's invention the ability to reuse the configuration information as stored in a memory, thereby increasing the adaptability of the system, and because Wise also taught a memory map for mapping hardware resources into the memory address (see Wise, col. 259, lines 10-25), and that his multiplexed network (see interconnection common box in Fig. 137) showed the points at which needed to be stored (see Wise, col. 262, lines 14-20), which was a suggestion of the desirability to save the configuration, such as the connection points, into a memory, and for doing so, provided a motivation. Wise also showed the storage of the configuration information (see Wise, the RAM organized into common control block in col. 265, lines 43-53; see also the common control block of Fig. 137)

7. As per claim 183, Wise further teaches the system of claim 182, wherein the configuration information provides a first system operating mode of the plurality of operating modes (see Wise, Fig. 137, operating in either carry-save multiplier, carry save adder or a carry save subtractor).

8. As per claim 184, Wise further teaches the system of claim 182, wherein the first plurality of heterogeneous computational elements are configured to generate a request for the second configuration information (see Wise, col. 64, lines 34-50, 'request').

9. As per claim 185, Wise further teaches the system of claim 182, wherein the memory comprises a third plurality of heterogeneous computational elements configured to perform a memory function in response to the configuration information (see functional mode of x[3,4] of Fig. 137).

10. As per claim 186, Wise further teaches the system of claim 182, wherein the configuration information is transferred to the system from a machine-readable medium or through a wireless interface (see Wise, microprocessor read port in col. 260, lines 32-35; see also RAM in col. 265, lines 43-53).

11. As per claim 187, Wise further teaches the system of claim 182, wherein the configuration information is embodied as a plurality of discrete information data packets or as a stream of information data bits (see Wise, Discrete cosine transform in col. 4, lines 1-11 for background; see also the data packets in col. 13, lines 53-57).

12. As per claim 188, Examiner holds that integrated circuit was already well known in the art at the time of the invention was made, thus the system shown in Wise must be embodied in an integrated circuit.

13. As per claims 189-190, Baxter further teaches wherein the computational units are organized in a configurable computing matrix and the computing matrix is coupled to a matrix interconnection network, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrices, each configurable computing matrix having a plurality of computational units (see Baxter, the interconnect Matrix in Fig. 1, see also the interconnect matrix for selectively routing in col. 10, lines 26-38). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use Baxter in Wise's invention for including the selectively routing the first and second configuration information as claimed because the use of Baxter could provide Wise the capability to reconfigure the processing elements at a predefined set of selection, thereby increasing the flexibility of the configurations, and because Wise also taught his interconnection network (see the common box in 137 was a multiplexed circuit, see Wise, col. 262, lines 14-19), which was a suggestion of the applicability of the selective routing, and for the above reasons, provided a motivation.

14. As per claims 191-193, Baxter further teaches wherein a first configured function of the configurable computing matrix is as a controller, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the

controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrices, wherein the controller is a RISC controller (see Baxter, Fig. 1, S machines, T machines, I/O T machines and I/O devices; see also col. 10, lines 26-38).

15. As per claim 194, Wise further teaches the system of claim 182, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information (see Wise, Fig. 137, interconnection network and col. 4, lines 21-23).

16. As per claim 195, Baxter further teaches system of claim 194, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions (see Baxter, col. 10, lines 26-38).

17. As per claim 196, Wise further teaches the system of claim 182, wherein the basic computational function is a logic function; and wherein the complex processing function is a digital signal processing function (see Wise, col. 4, lines 8-9 and the transforms; see also col. 30, lines 62-67).

18. As per claim 197, Wise further teaches the system of claim 182, wherein the basic computational function comprises bit level manipulation; and wherein the complex processing function comprises word level manipulation (see Wise, col. 40, lines 15-28).

19. As per claim 198, Wise further teaches the system of claim 182, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register (see Wise, Fig. 137, for adder, multiplier, subtract and I/O; see also col. 6, line 57 to col. 7, line 12).

20. As per claim 199, Wise further teaches the system of claim 198, wherein the basic computational function is a logic function; and wherein the complex processing function is a digital signal processing function (see Wise, col. 4, lines 8-9 and the transforms; see also col. 30, lines 62-67).

21. As per claim 200, Wise further teaches the system of claim 199, wherein the basic computational function comprises bit level manipulation; and wherein the complex processing function comprises word level manipulation (see Wise, col. 40, lines 15-28 and col. 30, line 62 to col. 31, line 4).

22. As per claim 201, Wise further teaches the system of claim 197, wherein the basic computational function is a logic function; and wherein the complex processing function is a digital signal processing function (see Wise, col. 4, lines 8-9 and the transforms; see also col. 30, lines 62-67).

23. As per claim 202, Wise further teaches the system of claim 196, wherein the first computational unit operates at a bit level; and wherein the second computational unit operates at a word level (see Wise, col. 40, lines 15-28 and col. 30, line 62 to col. 31, line 4).

24. As per claim 203, Wise further teaches the system of claim 202, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register (see Wise, Fig. 137, for adder, multiplier, subtract and I/O; see also col. 6, line 57 to col. 7, line 12).

25. As per claim 204, Wise further teaches the system of claim 182, wherein the basic computational function includes one of a group of linear operation, memory,

memory management, and bit level manipulation; and wherein the complex processing function is one of a group of fixed point arithmetic functions, floating point arithmetic functions, filter functions, and transformation functions (see Wise, Fig. 137, adder, multiplier; col. 4, lines 8-9, and col. 30, line 62 to col. 31, line 4).

26. As per claim 205, Wise further teaches the system of claim 204, wherein the basic computational function is a logic function; and wherein the complex processing function is a digital signal processing function (see Wise, col. 4, lines 8-9 and the transforms; see also col. 30, lines 62-67).

27. As per claim 206, Wise further teaches the system of claim 205, wherein the basic computational function comprises bit level manipulation; and wherein the complex processing function comprises word level manipulation (see Wise, col. 40, lines 15-28 and col. 30, line 62 to col. 31, line 4).

28. As per claim 207, Wise further teaches the system of claim 206, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register (see

Wise, Fig. 137, for adder, multiplier, subtract and I/O; see also col. 6, line 57 to col. 7, line 12).

29. As per claim 208, Wise further teaches the system of claim 207, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift (see Wise, Fig. 137, for adder, multiplier, subtract and col. 6, line 57 to col. 7, line 12).

30. As per claim 209, Wise further teaches the system of claim 182, further comprising a third interconnection network coupled to the first computational unit and the second computational unit, the third interconnection network sending the configuration information to the computational units (see Wise, Fig. 137 and col. 262, lines 14-42).

31. As per claim 210, Wise further teaches the system of claim 209, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network (see Wise, Fig. 137 and col. 262, lines 14-42, this would be based on the configuration, wherein the first network can be a denser than the second network).

32. As per claim 211, Wise further teaches the system of claim 182, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements, and the second interconnection network includes other multiplexers coupled to the second plurality of heterogeneous computational elements (see Fig. 137, multiplexers).

33. As per claim 212, Wise further teaches the system of claim 211, wherein the configuration information includes control signals to control the multiplexers (see Wise, Fig. 137 and col. 262, lines 14-42).

34. As per claim 213, it's rejected for the same reasons set forth above in claim 182.

35. As per claims 214-221, they are rejected for the same reasons set forth above in the corresponding claims 183-190.

36. As per claim 222, it is rejected for the same reasons set forth above in claim 182.

37. As per claims 223-245, they are rejected for the same reasons set forth above in the corresponding claims 191-213.

38. As per claim 246, the method of claim 246 is performed by the processor of claim 182. Consequently, claim 246 is rejected for the same reaons set forth in the rejection of claim 182 above.

39. As per claims 248, 249, 250, 251, they are rejected for the same reasons set forth above in the corresponding claims 183, 186, 189, 190.

40. As per claim 252, it is rejected for the same reasons set forth above in claim 182.

41. As per claims 253-275, they are rejected for the same reasons set forth above in the corresponding claims 191-213.

42. As per claim 276, the method of claim 276 is performed by the processor of claim 182. Consequently, claim 276 is rejected for the same reaons set forth in the rejection of claim 182 above.

43. As per claims 278, 279, 280, 281, they are rejected for the same reasons set forth above in the corresponding claims 183, 186, 189, 190.

44. As per claim 282, it is rejected for the same reasons set forth above in claim 182.

45. As per claims 283-305, they are rejected for the same reasons set forth above in the corresponding claims 191-213.

46. Claim 247 and 277 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise in view of Baxter, as applied to claims above, and further in view of Cohen et al. U.S. Patent No. 6,005,943 (hereinafter Cohen).

47. As to claim 247, neither Wise nor Baxter specifically showed the authorization to receive the configuration as claimed. However, Cohen taught authorization of the configuration (see fig.2, col.8, lines 5-52). It would have been obvious to one of ordinary skill in the art to use Cohen in Wise for including the authorization of the configuration as claimed because the use of Cohen could provide Wise the ability to accept the configuration information based on a predetermined set of requirements and restrictions, therefore increasing system security in Wise.

48. As per claim 277, it's rejected for the same reasons set forth above in claim 247.

Response to Arguments

49. Applicant's arguments with respect to claim 182-305 have been considered but are moot in view of the new grounds of rejection.

Conclusion

50. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
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